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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,218	11/25/2003	Shui-Ming Cheng	24061.149	6790
42717	7590	12/27/2004	EXAMINER	
HAYNES AND BOONE, LLP 901 MAIN STREET, SUITE 3100 DALLAS, TX 75202			WILLE, DOUGLAS A	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 12/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/722,218

Applicant(s)

CHENG ET AL.

Examiner

Douglas A Wille

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RW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-49 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-49 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>0304</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show the etch stop layer as described in the specification. Note that in paragraph [0025] the etch stop layer is described as being 180. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

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3. Claims 1 – 15, and 38 - 49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 44 and 47 show that the first FET has recessed or extended S/D and the second FET has recessed or extended S/D which can be any of the combinations of recessed/recessed, recessed/extended, extended/recessed and extended/extended. The last line states that the S/D regions are coplanar, which is inconsistent with the possibilities noted. Correction is required.

4. Claim 38 states that the FETs have SiC and SiGe in different S/D regions but the last line states that the S/D regions are free of SiC and SiGe, which is inconsistent. Correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 5 – 7, 11, 12 – 14, 38 and 44 are rejected under 35 U.S.C. 102(e) as being anticipated by Yeo et al.('815).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C.

102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the

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inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

7. With respect to claim 1 and 44, to the extent that the claims are understood, Yeo et al.('815) show CMOS structures with the NMOS and PMOS devices having protruding source/drain regions (see Figure 8 and paragraph [0049]).

8. With respect to claims 5, 6 and 7, Yeo et al.('815) show that the S/D regions can be either SiGe or SiC (paragraph [0049]).

9. With respect to claim 11, Yeo et al.('815) show a Si substrate (paragraph [0031]).

10. With respect to claims 12 - 14, Yeo et al.('815) show a strained source/drain (paragraph [0049]).

11. With respect to claim 38, Yeo et al.('815) shows the use of SiC and SiGe (paragraph [0049]).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claims 2, 16, 17, 18 - 20, 24 - 26, 40, 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al.('815) in view of Tao et al.

14. With respect to claims 2 and 40, Yeo et al.('815) do not describe the height of the gates but Tao et al. show (see column 4, line 61) that selection of gate height for a FET is a matter of device design. It would be obvious to design the gate height for the two different FETs with

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appropriate gate heights that would be different for different FETs due to different channel mobilities.

15. With respect to claims 16 and 45, Yeo et al.('815) show the basic structure and do not describe the height of the gates but Tao et al. show (see column 4, line 61) that selection of gate height for a FET is a matter of device design. It would be obvious to design the gate height for the two different FETs with appropriate gate heights that would be different for different FETs due to different channel mobilities. Note that Yeo et al.('815) describe isolation regions (paragraph [0047]).

16. With respect to claim 17, it would be a matter of design optimization to select the spacer width to adjust the LDD regions and different spacer widths would be obvious since different carrier statistics are involved in PMOS and NMOS devices.

17. With respect to claim 24, Yeo et al.('815) show a Si substrate (paragraph [0013]).

18. With respect to claims 25 and 26, Yeo et al.('815) show a strained source/drain (paragraph [0049]).

19. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al.('815) in view of Tao et al. and further in view of Shimizu et al.

20. With respect to claim 27, Yeo et al.('815) shows SiGe and SiC layers to provide strain and Shimizu et al. show that strain can be produced using a SiN film over the device. It would be obvious to use either the Yeo et al.('815) structure or the Shimizu et al. structure since similar results are obtained.

21. With respect to claims 18 - 20, Yeo et al.('815) show that the S/D regions can be either SiGe or SiC (paragraph [0049]).

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22. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al.('815) in view of Tao et al. and further in view of Yeo et al.('646).

23. With respect to claims 21 and 22, Yeo et al.('815) do not show the crystal orientation but Yeo et al.('646) show that (100) and (110) crystals can be used (paragraphs [0004] and [0007]). It would be obvious to use either orientation since they are known to be useful.

24. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al.('815) in view of Tao et al. and further in view of Baba et al.

25. With respect to claim 23, Yeo et al.('815) show a Si substrate (paragraph [0013]) but do not show a SOI substrate. Baba et al. show that a similar structure can be formed on a SOI substrate. It would be obvious to use a SOI substrate in the Yeo et al.('815) device to gain the advantages of the SOI structure.

26. Claims 3, 4, 28 - 31, 36, 41, 42 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al.('815).

27. With respect to claims 3, 4 and 46, it would be a matter of design optimization to select the spacer width to adjust the LDD regions and different spacer widths would be obvious since different carrier statistics are involved in PMOS and NMOS devices.

28. With respect to claims 28 and 41, Yeo et al.('815) show the CMOS structure with isolation regions and , it would be a matter of design optimization to select the spacer width to adjust the LDD regions and different spacer widths would be obvious since different carrier statistics are involved in PMOS and NMOS devices.

29. With respect to claims 29 – 31, Yeo et al.('815) show that the S/D regions can be either SiGe or SiC (paragraph [0049]).

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30. With respect to claims 36 and 42, Yeo et al.('815) show a strained source/drain (paragraph [0049]).

31. Claims 37 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al.('815) in view of Shimizu et al.

32. With respect to claims 37 and 43, Yeo et al.('815) shows SiGe and SiC layers to provide strain and Shimizu et al. show that strain can be produced using a SiN film over the device. It would be obvious to use either the Yeo et al.('815) structure or the Shimizu et al. structure since similar results are obtained

33. Claims 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al.('815) in view of Yeo et al.('646).

34. With respect to claims 32 and 33, Yeo et al.('815) do not show the crystal orientation but Yeo et al.('646) show that (100) and (110) crystals can be used (paragraphs [0004] and [0007]). It would be obvious to use either orientation since they are known to be useful.

35. Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al.('815) in view of Baba et al.

36. With respect to claims 34 and 35, Yeo et al.('815) show a Si substrate (paragraph [0013]) but do not show a SOI substrate. Baba et al. show that a similar structure can be formed on a SOI substrate. It would be obvious to use a SOI substrate in the Yeo et al.('815) device to gain the advantages of the SOI structure.

37. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al.('815) in view of Yeo et al.('646).

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38. With respect to claims 8 and 9, Yeo et al.('815) do not show the crystal orientation but Yeo et al.('646) show that (100) and (110) crystals can be used (paragraphs [0004] and [0007]). It would be obvious to use either orientation since they are known to be useful.

39. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al.('815) in view of Baba et al.

40. With respect to claim 10, Yeo et al.('815) show a Si substrate (paragraph [0013]) but do not show a SOI substrate. Baba et al. show that a similar structure can be formed on a SOI substrate. It would be obvious to use a SOI substrate in the Yeo et al.('815) device to gain the advantages of the SOI structure.

41. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al.('815) in view of Shimizu et al.

42. With respect to claim 15, Yeo et al.('815) shows SiGe and SiC layers to provide strain and Shimizu et al. show that strain can be produced using a SiN film over the device. It would be obvious to use the either the Yeo et al.('815) structure or the Shimizu et al. structure since similar results are obtained.

43. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al.('815) in view of Wu.

44. With respect to claim 39, Yeo et al.('815) shows that raised source/drains can be used to provide increased mobility of carriers (paragraph [0006]). Wu shows recessed source/drain regions in FETs (see cover Figure and column 3, line 66 et seq.) where operation speed of the devices is increased (column 2, line 54) and shows applications to ULSI (column 1, line 27) and requirements for interconnects (column 2, line 24). Since the two techniques of device formation

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have the same end result and since different formation methods are used it would be possible to tailor operation of devices to meet diverse application requirements and to use both types of devices for the same end use

45. Claims 47 - 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rodder et al. in view of Wu.

46. With respect to claims 47 and 48, Rodder et al. shows PMOS and NMOS devices formed with raised source/drain regions(column 2, line 42 et seq.) where the structure permits formation of small size devices (column 1, line 33). Wu shows recessed source/drain regions in FETs (see cover Figure and column 3, line 66 et seq.) where operation speed of the devices is increased (column 2, line 54) and shows applications to ULSI (column 1, line 27) and requirements for interconnects (column 2, line 24). Since the two techniques of device formation have the same end result and since different formation methods are used it would be possible to tailor operation of devices to meet diverse application requirements and to use both types of devices for the same end use.

47. With respect to claim 49, it would be a matter of design optimization to select the spacer width to adjust the LDD regions and different spacer widths would be obvious since different carrier statistics are involved in PMOS and NMOS devices.

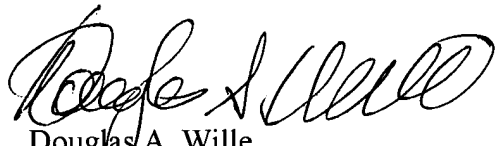
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas A. Wille whose telephone number is (571) 272-1721. The examiner can normally be reached on M-F (6:15-2:45).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Douglas A. Wille
Primary Examiner